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LC-FREE CMOS OSCILLATOR EMPLOYING TWO-DIMENSIONAL TRANSMISSION LINE

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*Abstrac*t - **A compact, fully integrated 5.2 GHz CMOS oscillator based on 0.25μm 1P5M foundry technology is presented. The recently proposed two-dimensional transmission line, called complementary-conducting-strips (CCS), replaces the conventional inductor-capacitor tank circuit, resulting in a first-pass design for the CMOS oscillator, of which the simulated and measured power level and oscillation frequency agree to within 1%.**

Keywords **- Soc, rfic, cmos, oscillator, two-dimensional transmission line, complementary-conducting-strips (CCS) transmission line**

I. INTRODUCTION

Communication system-on-chip (SOC) plays a key role for the proliferation of miniaturized products available in the market today. The trend toward the system chip integration of wireless RF equipments and devices is also inevitable in view of overall costs and labors of making them [1]. When developing communication SOC's, RFIC (radio-frequency integrated circuit) in particular, designers and managers have to decide what technology should be applied; whether III-V compound device or silicon-based IC is preferred. This paper adopts the silicon RF CMOS integration of wireless communication IC's [1], since mixed-signals circuits can be integrated on the same chip. Despite that NMOS or PMOS have low breakdown voltages, transmission line and inductors are highly lossy, and substrate couplings are great concerns in CMOS technology, CMOS RFIC has increasingly gained popularity among RF designers [2]. One of the important RFIC building blocks is oscillator or voltage-controlled oscillator (VCO). To achieve low phase noise, tuned oscillator is desirable. Thus high-performance oscillator often needs high-Q (quality factor) resonator, which is not available in modern CMOS technology. If high-Q resonators are removed from monolithic integration, issues such as reliability and repeatability arise.

To date CMOS cross-coupled tuned L-C oscillator is a mature choice for fully monolithic integration of oscillator, in which the cross-coupled CMOS pairs create sufficient amount of negative conductance to compensate the losses of the low-Q LC tank circuit [3]. Accurate design of on-chip inductors and capacitors is therefore of primary importance, since RF CMOS foundry often lacks support of scalable inductors and capacitors with very limited choices. Another problem is the repeatability of the inductors and capacitors; the characteristics of these passive components may vary from lot to lot and wafer to wafer. As the operating frequency increases, the behavior of inductor is more distributive rather than lumped, as it was initially intended. This further complicates the monolithic CMOS oscillator design at higher microwave frequencies.

This paper presents a CMOS RFIC guided wave structure that is fully compatible with the existing CMOS fabrication without special needs for mask change or process tuning. The proposed guiding structure has the following features: 1) The characteristics impedance of the transmission line is controlled by the unit-cell pattern in contrast to the conventional one-dimensional transmission line whose characteristics impedance is adjusted by the width of transmission line, when substrate height had been defined by foundry process; 2) The unit-cell of transmission line, having its transverse and longitudinal dimensions much larger than the height of the transmission line, makes the transmission line a two-dimensional structure, although it can be modeled one dimensionally; 3) The coupling of the adjacent cells is negligible, thereby a very compact layout of transmission line circuit is achieved.

When incorporating the proposed two-dimensional CMOS transmission line structure into the CMOS oscillator design, the LC tank of the conventional, tuned, cross-coupled CMOS oscillator can be replaced by the proposed transmission line of appropriate length as shown in Fig.1. Since the frequency of oscillation is determined primarily by the length of transmission line, not the parallel combination of inductor and capacitor, the sensitivity of oscillating frequency to process variation is largely reduced.

In the following, Section II reports the design of two-dimensional transmission line in a 0.25μm 1P5M CMOS foundry process. Section III describes the LC-free CMOS oscillator design. Section IV compares the simulated and measured results. Section V concludes the paper.

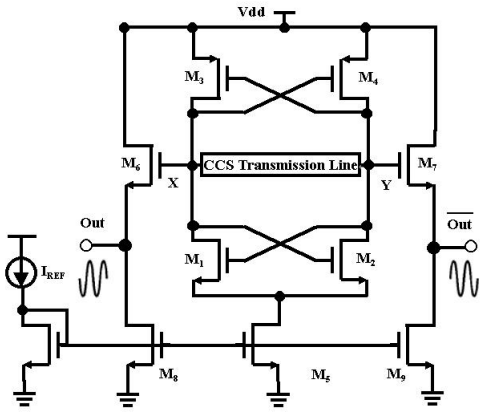

Fig. 1. CMOS oscillator employing CCS TL

II. TWO-DIMENSIONAL TRANSMISSION LINE: THE COMPLEMENTARY-CONDUCTING STRIPS (CCS) TL

Transmission lines such as microstrip and coplanar waveguide (CPW) have been widely applied in GaAs or III-V-based IC's, since the semi-insulating substrates are low-loss dielectric materials and the resultant quality factors of microstrips and CPW's have acceptable Q values. This is, however, not the case for CMOS RFIC. The finite substrate losses seriously limit the Q-factor of a typical CMOS microstrip line or CPW above the CMOS SiO2 layer to approximately six-to-ten, or even worse, depending on how the transmission line is actually built. In CMOS process, much thinner metal layers than those incorporated in III-V-based ICs are typical in standard foundry processes. This makes improvement of Q-factor of CMOS transmission line a difficult task unless the process is modified. If one raises the back plating layer of a typical CMOS microstrip to one of the five metal layers of the 1P5M CMOS technology, the resultant new thin-film microstrip will show shrinking cross-sectional geometry. Thus microstrip of much smaller width will have the same characteristic impedance as that of a much wider microstrip on CMOS substrate. The penalty of doing this is the substantial increase in attenuation constant, which can produce disastrous electric performances. Nevertheless the thin-film microstrip is still attractive [4], since certain miniaturized passive components can be integrated. This paper proposes a new guiding structure that compromises guided-wave losses and size, and results in flexibility of current handling capability and choice of characteristic impedance.

Fig.2 illustrates the unit cell of one example incorporating the proposed transmission line in the LC-free CMOS oscillator. On the bottom layer is the connected unit cell as shown by the crosshatched surface, which consists of the lowest M1 and M2 layers of the 1P5M CMOS process. On the top surface of the unit cell is patterned to make a 50-Ωtransmission line for the particular application. When viewed from the cross section of the unit cell, the unit cell comprises of a raised CPW and a thin-film microstrip connected in series. The ground planes of the raised CPW and that of the thin-film microstrip are connected on the bottom metallic plane. The proposed transmission line is the series connection of such unit cells, which may have signal paths in straight line or bent fashions; thus theses cells constitute the complete guiding structure in periodic arrangement. When looking into the top surface, we observe the top metal layer and bottom metal surface complement each other; therefore we name the proposed guiding structure the complementary conducting strips (CCS) transmission line, which has been incorporated into various miniaturized RFIC designs operated at microwave and millimeter-wave frequencies. The CCS transmission line is a periodical array, along which the guided wave experiences perturbation in the longitudinal direction. Therefore the proposed guiding structure is two-dimensional, increasing degrees of freedom for designing transmission line of various characteristic impedance and current handling capability. As will become clearer in the next section, very compact layout of transmission line equivalent of LC-tank circuit can be obtained owing to the fact that the adjacent cells have negligible coupling, typically well below –20 dB of coupling.

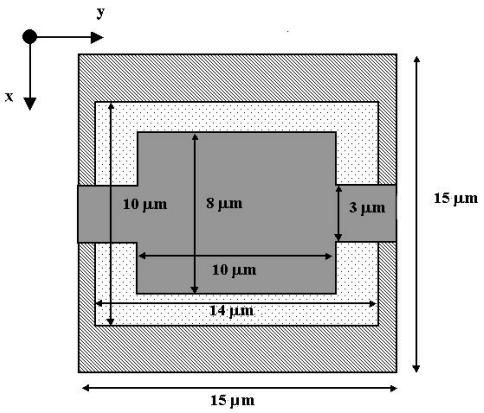

Fig. 2. Unit cell of the Complementary Conducting Strip (CCS)

III. LC-FREE CMOS OSCILLATOR DESIGN

As shown in Fig.1, complementary cross-coupled transistors, M_1, M_2, M_3, and M_4, form dual positive feedback loops and generate negative conductance, which cancels the losses of the transmission line resonator. Proper sizing of transistors, NMOS 100/0.25 and PMOS 160/0.25, assures sustained oscillation. At 5.2 GHz, the capacitive loading of transistors to the resonator is fairly large and the length of transmission line resonator is reduced from half wavelength when free of loading effect to approximately one sixth of guided wavelength. Fig.3 is the photo of the CMOS oscillator, on top of which is a 15 by 15 CCS (complementary conducting strips) array acting as a transmission line resonator, occupying 225 by 225 μm^2 area. The bottom plate of the adjacent cells connects the unit cells, thus rendering very compact layout. Total active chip area is 500 µm by 600 µm, including all the external pads.

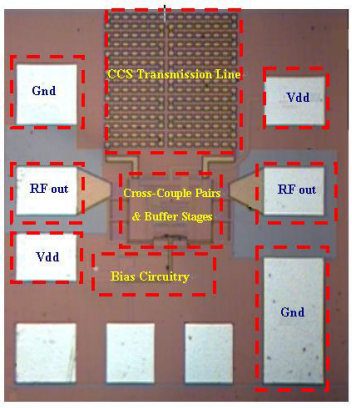

Fig. 3. Chip photograph of the fabricated oscillator

IV. MEASURED RESULTS

The bias condition for the oscillator core is set at 20 mA from a 3 V supply. A microwave probe station with ground-signal and signal-ground probes is applied to the differential RF output ports. The output signals are attenuated before reaching the probes to prevent loading to the oscillator. An HP 8565E spectrum analyzer is used to measure the oscillation frequency and the output power. The measured insertion loss from the probes to the spectrum analyzer is 1.53 dB at 5.2 GHz. Therefore, the measured power on the spectrum analyzer should be compensated by the probe losses. Fig.4 shows the measured output power spectrum of one RF output. The oscillation frequency is 5.2 GHz, which is 40 MHz away from the simulated frequency, and the output power is –25.3 dBm against –26.0 dBm in theory. Figure 5 plots the preliminary result for the single sideband (SSB) phase noise. The phase noise is –96 dBc/Hz at 1MHz offset from the carrier.

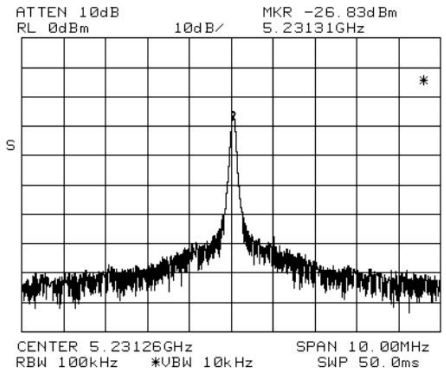

Fig. 4. Measured single-ended output power spectrum

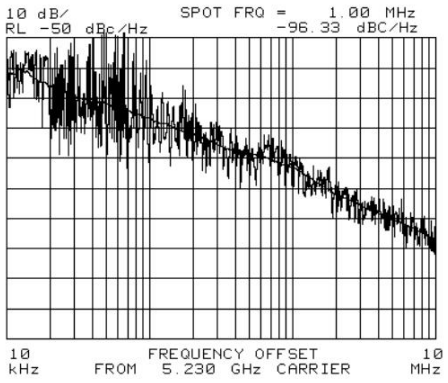

Fig. 5. Measured SSB phase noise

V. CONCLUSION

This paper presents a first-pass design approach to the full integration of CMOS oscillator incorporating the recently proposed two-dimensional complementary-conducting-strips (CCS) transmission line (TL). Power spectrum measurement shows excellent agreements with the simulated results. Although the phase noise measurement is still illusive as the result of equipment setup, the improved CCS TL version may reduce the phase noise in near future.

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